WEST Search History

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☐	L27	l20 or l21 or l22 or l23 or l24 or l25 or l26	4720
☐	L26	370/503.ccls.	1555
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☐	L15	((adjust$4 or align$4 or realign$4) near3 data near3 skew$4)	153
☐	L14	(realign$8 same validat$4 same (data near2 (receipt or receiv$4)))	2
☐	L13	(realign$8 near5 validat$4 near5 (data near2 (receipt or receiv$4)))	0
☐	L12	(realign$8 near5 (after near2 validat$4) near5 (data near2 (receipt or receiv$4)))	0
☐	L11	l2 same control$4	10
☐	L10	L6 same (misalign$7 or realign$7 or align$7)	9
☐	L9	L6 and (misalign$7 or realign$7 or align$7)	23
☐	L8	L6 and ((misalign$7 or realign$7 or align$7) near3 skew$4)	0
☐	L7	L6 same ((misalign$7 or realign$7 or align$7) near3 skew$4)	0
☐	L6	((concurrent$4 or simultaneous$4) near3 (transmit$4 or transfer$4 or send$4) near3 (encod$4 or cod$4) near3 data)	148
☐	L5	L3 same (realign$4 or align$7)	2

☐	L4	L3 same realign$4	1
☐	L3	L1 with (parallel$4 near3 (transfer$4 or transmit$4 or send$4 or communicat$4))	22
☐	L2	L1 same (parallel$4 near3 (transfer$4 or transmit$4 or send$4 or communicat$4))	47
☐	L1	(data near3 skew$4)	2830

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L14: Entry 2 of 2 File: USPT Apr 7, 1998

DOCUMENT-IDENTIFIER: US 5737371 A
TITLE: Realignment of data stream from an optical disk

Detailed Description Text (3):
FIG. 3 is a block diagram of an optical drive unit 300 of the present invention which reads/writes data from/to an optical disk 200 and transmits/receives the data to/from a host device 10. The drive unit 300 includes an optical head 302 for directing a laser beam onto a surface of the disk 200 and detecting the light reflected from the surface, a converter 304 for converting the analog signal from the detector into a digital data stream representative of the data read back from the disk 200, a digital read channel, an input/output interface 306 through which data and commands are exchanged with the host 10 and a microprocessor 308 to control all aspects of the operation of the drive unit 300. The drive unit 300 further includes a data realignment module 310, a data divider 312 and positive and negative shift registers 314 and 316, respectively; the data realignment module 310 has a resync misalignment detector 700, validated resync misalignment module 800, an unvalidated resync misalignment module 900, a sync misalignment detector 1200 and a realignment controller 1300, 1400, all of which will be described in detail below. Modules 700 and 1200 are both connected to both of the registers 314 and 316 to permit proper misalignment detection and correction whether the alignment bit is represented by a positive transition or a negative transition. Although the present invention will be described in terms of the positive transitions being processed through the positive register 314 and the negative transitions being processed through the negative register 316, the present invention contemplates the opposite mode of processing as well.

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L14: Entry 1 of 2 File: USPT Mar 18, 2003

DOCUMENT-IDENTIFIER: US 6536025 B2
TITLE: Receiver deskewing of multiple source synchronous bits from a parallel bus

Detailed Description Text (12):
After the data and strobe signals have been translated by the line receivers of the receiver IC die, the bit-to-bit timing variation among the different data signals is reduced using the deskew circuitry, before each group of N bits are captured and validated using their respective transition in the strobe signal. This means that the predetermined delay that is provided by each delay element 408 (See FIG. 4) has been previously fixed to an amount that realigns the center of each bit interval in a data signal with respect to a particular transition in the strobe signal. See FIG. 6 for an exemplary timing diagram of the received data signals D1, D2 and D3 and the deskewed/realigned data signals D1', D2' and D3'. After this realignment, the transition in the strobe signal S' may be used to latch the logic value that appears in each deskewed data signal D1', D2' or D3'.

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L11: Entry 10 of 10 File: USPT Jan 20, 1987

DOCUMENT-IDENTIFIER: US 4638381 A
TITLE: Storage of digitized video images on disk

CLAIMS:

1. A digital data deskewing circuit for use with a parallel transfer digital disk drive having a plurality of coaxially arranged magnetic disks rotating together at a constant speed, a plurality of digital data transmission channels and read/write heads magnetically coupling the channels to the disks, respectively, a master clock controlling writing on the respective disks a number of digital words, bytes or other digital data bit groups, said groups being written on each disk as a serial stream of bits, during reading of the streams from the disks said drive providing a bit read clock pulse train for each channel for defining the bits and a sync data bit grouping derived from the disk and preceding valid digital data, said clock pulses sometimes being out of synchronism with each other such that the data bits are skewed in time relative to each other during readout of the disks, said disk drive issuing an index pulse for each disk revolution sectors pulses marking each disk sector,

deskewing circuit means comprising master sequencer means referenced to the index and sector time base of the disk drive and operative to provide clock pulse signals for serial bit stream outputs from all channels at the same time,

each channel including serial-to-parallel converter means having a data input for serial bits from a disk and an input for said bit read clock of the channel, said converter having a predetermined number of parallel bit outputs,

sync detector means coupled to said parallel bit outputs of said converter means, detection of said sync data indicating that serial bits composing valid data follow,

digital latch means having parallel bit inputs coupled to the respective parallel bit outputs of said converter means and having corresponding outputs and a clock pulse input which clock rate is a fraction of the bit read clock rate to said serial-to-parallel converter, so that for every latch means clock said predetermined number of bits will be transferred from said converter to said latch means,

first-in, first-out (FIFO) memory means having parallel bit inputs coupled to corresponding outputs of said latch means, having corresponding parallel bit outputs and having an input clock that is such fraction of said read clock rate and having an output clock supplied by said master sequencer means for controlling the rate at which parallel bits are transferred together out of said FIFO memory means,

parallel-to-serial converter means having parallel bit inputs coupled to corresonding outputs of said FIFO memory means and having a bit rate output control clock supplied by said master sequencer and having an output for serially arranged

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L11: Entry 8 of 10 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243824 B1

** See image for Certificate of Correction **

TITLE: Array disk subsystem

Detailed Description Text (36):

Referring now to FIG. 8, a description will be given of an embodiment according to the present invention in which subdivided data items are sent from a host (CPU 1) to the system. The CPU 1 splits a data item into subdata items in a certain unit to send the subdata items to the DCU 2 in a parallel manner. The DCU 2 achieves a control operation on data items in the disk subsystem. In a write operation, the parallel data items thus received from the CPU 1 are stored in the data buffer 3 under control of the DCU 2 without changing the data items. The DCU 2 produces ECCs for these data items from the CPU 1 to similarly transfer the ECCs to the data buffer 3. The data buffer 3 absorbs the difference or skew with respect to time of the data items and the ECCs transferred in a parallel fashion to adjust timings (associated with the seek time and the rotation latency) for the write operations on the data disks 6a to 6d. When a free path exists for the data disks 6a to 6d, the associated subdata items and ECCs are transferred thereto and to the ECC disk 7. In a read operation, the respective subdata items are read from the related data disks 6a to 6d to be transferred in parallel into the data buffer 3. Absorbing the skew with respect to time of the respective subdata items, the data buffer 3 determines an appropriate transfer timing (for a free path) to the CPU 1 so as to send the subdata items thereto. Also in this embodiment, the backup method described in conjunction with the embodiments 4 and 5 may be employed.

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L11: Entry 2 of 10 File: USPT Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6665499 B2
** See image for Certificate of Correction **
TITLE: Parallel optical transmission/reception module

Brief Summary Text (15):
When the skew data reception unit is assembled in a parallel optical transmission module, the parallel data signals may be transmitted after the reception of the parallel pattern signals are confirmed. The transfer after the confirmation serves to inspect the connection between the parallel optical transmission and reception modules by optical transmission paths such as optical fibers. In this case, it is possible to apply Class 1 regulation in the laser safety regulation to the transmission of optical pattern signals while applying Class 4 regulation to the transmission of optical data signals, so that larger power may be obtained according to Class 4 regulation for data transmission, and at the same time, reduced requirements can be applied to handling of the modules according to Class 1 regulation. It is possible to realize an open fiber control system.

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L11: Entry 3 of 10 File: USPT Nov 11, 2003

DOCUMENT-IDENTIFIER: US 6647506 B1
TITLE: Universal synchronization clock signal derived using single forward and reverse direction clock signals even when phase delay between both signals is greater than one cycle

Detailed Description Text (208):
Thus, as described herein, a synchronous bus system 10 of the present invention can support the transfer of data and control information among a master device 12 and a number of slave devices 14. The synchronous bus system 10 includes a two-segment clock line 28, synchronization clock circuitry 22 in all devices, and clock-data skew correction circuitry in only slave devices 14. Clock line 28 can run physically parallel to a data bus for transmitting data between the devices. Clock line 28 extends from a clock source 26, connects to each of master device 12 and slave devices 14 in a forward direction, turns around at a distal end of the data bus, and connects again to each of master device 12 and slave devices 14 in a reverse direction. Synchronization clock circuitry 22 allows all devices to derive a universal synchronization clock signal (comprising a transmission and reception signal components) that is used as a reference clock in each devices. Skew correction circuitry 24 compensates or corrects for clock-data skew caused by any mismatch between clock line 28 and the data bus. Skew correction circuitry 24 also synchronizes all data input/output transactions to the universal synchronization clock signal. As a result, master device 12 can readily communicate with all slave devices 14, even if clock-data skew exists in the synchronous bus system 10.

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L11: Entry 4 of 10 File: USPT Nov 11, 2003

DOCUMENT-IDENTIFIER: US 6647027 B1
TITLE: Method and apparatus for multi-channel data delay equalization

Detailed Description Text (12):
The present invention provides a method and apparatus for equalization of relative delay skew among different data channels. This equalization may be applied to various parallel data transfer systems, such as SCSI bus systems. The present invention provides delay equalization on a per channel basis. This equalization mechanism is employed for a number of reasons. For example, the control of delay skew between pairs of SCSI cables is limited by mechanical means of cable manufacturing. Other control means for delay skew between two protocol chips, such as a host and target, and among 27 data channels for two buses is limited by the accuracy of various computer aided design tools for layout to parasitic extraction. The present invention recognizes that the integrated circuit packages used for SCSI devices, such as ball grid array (BGA), exhibit pin-to-pin delay on the order of 30 pico seconds to 50 pico seconds. The back-plane boards exhibit delay skew among pairs of signal traces presently in the order of a nanosecond. Also recognized is the change of load in devices, such as RAUD boxes, demands automated or semi automated equalization on a per channel basis.

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L10: Entry 1 of 9 File: USPT Mar 12, 2002

DOCUMENT-IDENTIFIER: US 6356555 B1
TITLE: Apparatus and method for digital data transmission using orthogonal codes

Detailed Description Text (35):
The concept in alignment is to adjust variable delays imposed at the site of each transmitter prior to transmission of a barker code so as to compensate for different propagation delays from each transmitter site such that the barker code from each subscriber transmitter trying to align arrives at the head end receiver during the same gap. When the variable delays at each subscriber transmitter are adjusted properly, each subscriber will be said to be in alignment so that the signals encoding the symbols that are simultaneously transmitted on the shared data path 24 will all be transmitted with the same frame timing.

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L4: Entry 1 of 1 File: USPT Jul 6, 1999

DOCUMENT-IDENTIFIER: US 5920704 A
TITLE: Dynamic routing switch apparatus with clocked signal regeneration

Brief Summary Text (30):
The problem with the unbuffered, asynchronous method is that the data transmission pulses passing through each switch stage are not reshaped or realigned by a relatching process. As the signals pass through multiple switch stages, the original pulse shape can get distorted. Also, data that is transferred in parallel (such as byte wide transfers) can experience skew amongst the parallel data bits, because the parallel lines are not realigned at every stage of the network. These two problems of pulse distortion and skewing limit the frequency of the transmission and the number of stages of network that can be traversed before the pulses become too distorted or skewed to be reliable.

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